Intel® 855GME Embedded Chipset Graphics and Memory Controller Hub (GMCH)

Specification Update Addendum

December 2003

Notice: The Intel® 855GME Embedded Chipset Graphics and Memory Controller Hub (GMCH) may contain design defects or errors known as errata that may cause the product to deviate from published specifications. Current characterized errata are documented in this specification update.

Order Number: 274004-002

Contents

Revision History

Date	Version	Description
December 2003	002	Additional graphic resolutions updated
October 2003	001	Initial release.

Preface

This document is an addendum to the Intel 855GME Chipset Graphics and Memory Controller Hub (GMCH) specification update. This spec update addendum is intended for embedded designs ONLY. It contains Specification Changes, Errata, Specification Clarifications, and Documentation Changes.

This document is an update to the specifications contained in the documents listed in the following Affected Documents/Related Documents table. It is a compilation of device and document errata and specification clarifications and changes, and is intended for hardware system manufacturers and for software developers of applications, operating system, and tools.

Information types defined in Nomenclature are consolidated into the specification update and are no longer published in other documents.

This document may also contain information that was not previously published.

Affected Documents/Related Documents

Title	Order
Intel® 855GM/855GME Chipset Graphics and Memory Controller Hub (GMCH) Datasheet	252615-002

Nomenclature

Errata are design defects or errors. These may cause the Intel® 855GME Embedded Chipset Graphics and Memory Controller Hub (GMCH)'s behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

Specification Changes are modifications to the current published specifications. These changes will be incorporated in any new release of the specification.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in any new release of the specification.

Documentation Changes include typos, errors, or omissions from the current published specifications. These will be incorporated in any new release of the specification.

Note: Errata remain in the specification update throughout the product's lifecycle, or until a particular stepping is no longer commercially available. Under these circumstances, errata removed from the specification update are archived and available upon request. Specification changes, specification clarifications and documentation changes are removed from the specification update when the appropriate changes are made to the appropriate product specification or user documentation (datasheets, manuals, etc.).

Summary Table of Changes

The following table indicates the errata, specification changes, specification clarifications, or documentation changes which apply to the Intel® 855GME Embedded Chipset Graphics and Memory Controller Hub (GMCH) product. Intel may fix some of the errata in a future stepping of the component and account for the other outstanding issues through documentation or specification changes as noted. This table uses the following notations:

Codes Used in Summary Table

Stepping

X:	Errata exists in the stepping indicated. Specification Change or Clarification that applies to this stepping.
(No mark) or (Blank box):	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.

Page

(Page):	Page location of item in this document.

Status

Doc:	Document change or update will be implemented.
Fix:	This erratum is intended to be fixed in a future step of the component.
Fixed:	This erratum has been previously fixed.
NoFix:	There are no plans to fix this erratum.
Plan Fix:	This erratum may be fixed in a future stepping of the product.

Row

|	Change bar to left of table row indicates this erratum is either new or modified from the previous version of the document.

Errata

No.	Steppings			Page	Status	ERRATA
	#	#	#			
1.	A2			9	Fixed.	Display may flicker when integrated graphics and ECC support are enabled.

Specification Changes

No.	Steppings		Page	Status	SPECIFICATION CHANGES
	#	#			
					None for this revision of this specification update.

Specification Clarifications

No.	Steppings			Page	Status	SPECIFICATION CLARIFICATIONS
	#	#	#			
1.	A2			11	No Fix	Graphics Limitations Using ECC DIMM Memory

Documentation Changes

No.	Document Revision	Page	Status	DOCUMENTATION CHANGES
				None for this revision of this specification update.

Identification Information

Component Identification via Programming Interface

The Intel® 855GME Embedded Chipset Graphics and Memory Controller Hub (GMCH) may be identified by the following register contents.

Stepping	Vendor ID[1]	Device ID[2]	Revision Number[3]
A2	8086h	3580h	02h

NOTES:
1. The Vendor ID corresponds to bits 15-0 of the Vendor ID Register located at offset 00-01h in the PCI function 0 configuration space.
2. The Device ID corresponds to bits 15-0 of the Device ID Register located at offset 02-03h in the PCI function 0 configuration space.
3. The Revision Number corresponds to bits 7-0 of the Revision ID Register located at offset 08h in the PCI function 0 configuration space.

Markings

The Intel® 855GME Embedded Chipset Graphics and Memory Controller Hub (GMCH) may be identified by the following component markings.

Stepping	Tracking Code	Notes
A2	S-Spec SL72L	82855GME GMCH Top Marking: RG82855GME

Errata

1. Display may flicker when integrated graphics and ECC support are enabled.

Problem: Memory with ECC enabled requires more system memory resources. This will cause the Integrated graphics engine to have less memory bandwidth for access to the graphics frame buffer.

Implication: Display flicker and flashing may occur when ECC is enabled under high-resolution graphics modes.

Workaround: System BIOS workaround is required to allow integrated graphics more access time to memory. Contact your BIOS vendor for latest update.

Status: Fixed.

Specification Changes

None for this revision of this specification update.

Specification Clarifications

1. Graphics Limitations Using ECC DIMM Memory

Memory with ECC enabled requires more system memory resources. This will cause the Integrated graphics engine to have less memory bandwidth for access to the graphics frame buffer.

A system BIOS workaround is required to allow integrated graphics more access time to memory. Contact your BIOS vendor for latest updates.

SO-DIMM memory with ECC enabled is not supported.

DIMM memory with ECC enabled will be supported under the following display configurations for non-mobile configurations (see Table 1).

Table 1. Supported Internal Graphics Display Configuration with ECC Enabled

Graphics Core (Minimum Frequency)	200 MHz
Memory (Minimum Frequency)	266 MHZ
FSB (Minimum Frequency)	400 MHz
Display Usage	Dual Independent Display
Dual Pipe Independent (Maximum Display Resolution)	Contact your local Field Representative for supported Dual Independent Display configurations
Single Pipe Independent (Maximum Display Resolution)	1600 x 1200, 2 bytes per pixel (BPP), 85 Hz (DCLK=56.25MHz) on CRT/DVO 1600 x 1200, 4 BPP, 85 Hz (DCLK=56.25MHz) on CRT/DVO 1600 x 1200, 4 BPP, 60 Hz (DCLK=65MHz) on LVDS
LVDS Support	Yes
ADD card Support	Yes
Display Concurrency	1 Plane Per Pipe + Cursor + Overlay
SSC Support	No

Documentation Changes

None for this revision of this specification update.

§ §